REMARKS

Claims 1, 2 and 4-9 are pending in this application. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with Markings to Show Changes Made."

Rejections under 35 USC §103(a)

Claims 1, 2, 4, 9 and 5-8 were rejected under 35 USC §102(b) as being obvious over Cantell et al (U.S. Patent No. 6,255,179) in view of excerpt from Van Zant, Microchip Fablication, 4th ed, McGraw Hill: New York, 2000, pp 172-173, 179-182.

Applicant respectfully traverses this rejection.

Claims 1 and 5 have been amended to recite "implanting arsenic ions into the wiring using the resist pattern as a mask." This amendment is supported in the first to third full paragraphs on page 6 of the present specification.

Cantell et al discloses: "To form the source and drain regions on the FET, dopants such as boron, and phosphorous are implanted into the water" (column 1, lines 27-28). Cantell et al does not teach or suggest that arsenic (As) is used as a dopant. A mass number of As is larger than those of the other dopants. Therefore, a problem may arise when As is used as a dopant. (Please see page 6, lines 22-24 of the specification.) Therefore, a person of ordinary skill in the art would not be motivated to use arsenic (As) as a dopant.

Van Zant is cited for allegedly disclosing that rapid thermal processing is advantageous for reducing thermal budget. Such disclosure, however, does not remedy the deficiencies of Cantell et al.

For at least these reasons, claims 1 and 5 patentably distinguish over Cantell et al and Van Zant. Claims 2, 4 and 9, depending from claim 1, claims 6-8, depending from claim 5, also patentably distinguish over Cantell et al and Van Zant for at least the same reasons.

Thus, the 35 USC §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE S.N. 09/995,575

IN THE CLAIMS:

Claims 1 and 5 have been amended as follows:

1. (Twice Amended) A method for manufacturing a semiconductor device, comprising the steps of:

forming a wiring comprising silicon on a surface of a semiconductor substrate;

covering part of the wiring with a resist pattern;

implanting arsenic ions into the wiring using the resist pattern as a mask;

removing the resist pattern;

thinning the wiring by removing a surface layer of the wiring to a depth of at least 5 nm; and

forming a metal silicide film on a surface of the wiring by causing reaction between a surface layer of the thinned wiring and a refractory metal which reacts with silicon to form silicide,

wherein the wiring thinning step comprises the steps of:

oxidizing the wiring, using a rapid thermal processing ~~apparatus~~, beginning on an upper surface thereof down to a predetermined depth; and

removing an oxidized section of the wiring oxidized in the oxidizing step.

5. (Twice Amended) A method for manufacturing a semiconductor device, comprising the steps of:

forming wiring comprising silicon on a surface of a semiconductor substrate;

covering part of the wiring with a resist pattern;

implanting arsenic ions into the wiring using the resist pattern as a mask;

removing the resist pattern;

oxidizing the wiring, using a rapid thermal processing ~~apparatus~~, beginning on an upper surface thereof down to a predetermined depth;

removing an oxidized section of the wiring oxidized in the oxidizing step and thereby thinning the wiring; and

forming a metal silicide film on a surface of the wiring by causing reaction between a surface section of the thinned wiring and a refractory metal which reacts with silicon to form silicide.